ADATA Technology Corp.

Half mSATA SSD Module Datasheet

IXM26-XXXGXX

1GB, 2GB, 4GB, 8GB, 16GB, 32GB, 64GB

Version 0

Document Number: R21-0245

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Revision History

Revision No.	History	Draft Date	Remark	Editor
0	Formal release	Jul. 16, 2013		Andy Lin

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1.0 Product Description

1.1 Product Overview

Taking the advantages of NAND flash memory, Solid State Drive (SSD) provides better solutions on durability, performance, and power efficiency over traditional hard disk drives. Employing dynamic/static wear-leveling technology to maximize device mean time between failures (MTBF), The SSD solutions are your best choice on wide-ranged mobile computing devices and consumer electronic products. With Half mSATA form factor (JEDEC MO-300B) or customized module form factor, The ADATA IXM26 Module SSD offers capacities from 1GB to 64GB using (SLC/MLC) NAND type flash memories.

1.2 Application Fields

- Industrial PC and Thin Client
- Ticketing, Examining and Testing Machine
- Military, Health and Automatic Equipment
- Other machines and Equipment with mSATA interface slots on mother-board

1.3 Features

- Capacity: 4GB, 8GB, 16GB, 32GB (MLC)
  1GB, 2GB, 4GB, 8GB, 16GB, 32GB (SLC)
- Compliance with JEDEC MO-300B Standard.
- Fully compatible with standard SATA I/II specifications
- Implement dynamic/static wear-leveling algorithm and ECC (Error Correction Code)
- Low power consumption
- No noise and no latency
- Shock resistance and anti-vibration
- Built-in Short Circuit Protection
- Built-in Thermal Shutdown Function
- Built-in Current Limit Function
- Fully compatible with OS that supports SATA standard (Windows XP, Vista, Window 7, Mac OS, and Linux)
- RoHS compliant

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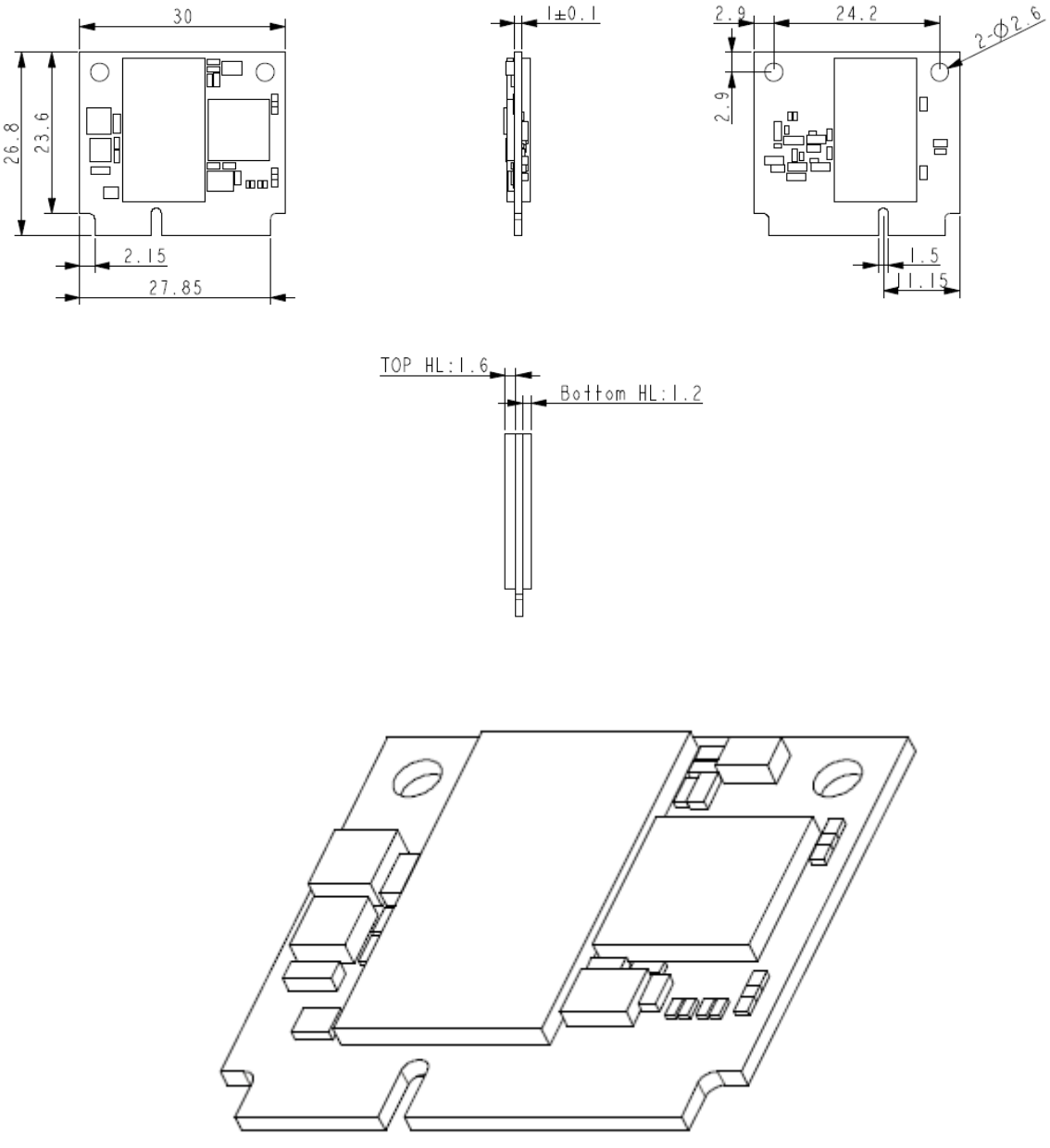
2.0 Mechanical Specification

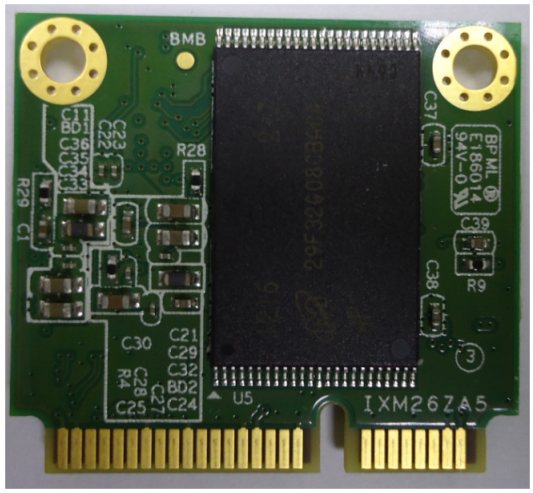
2.1 PCBA Dimensions



[Figure 2-1] PCBA Dimensions

2.2 Physical dimensions and Weight

Dimensions	Size	26.8 x 30 x 3.8mm (L x W x H)
	Weight	4±1g
	Connector	Standard mSATA golden finger

IXM26	
Front	**Back**
	

”All product specifications not covered in this document (electrical performance, appearance, etc.) are in accordance with ADATA’s defined norms and standards. “

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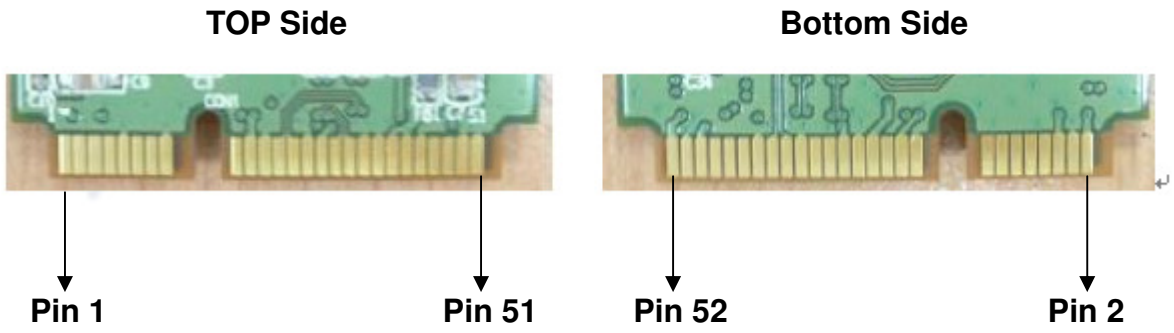
3.0 Electronic Specification

3.1 mSATA SSD Module Interface Connector and PIN Assignment

Device Connector: mSATA type 52 pin



Pin#	Assignment	Description	Pin#	Assignment	Description
1	N/A	No Connect	27	GND	System ground
2	+3.3V	DC 3.3V input source	28	Reserved	Reserved pin
3	N/A	No Connect	29	GND	System ground
4	GND	System ground	30	N/A	No Connect
5	N/A	No Connect	31	SATA_RX-	SATA Differential RX-
6	Reserved	Reserved pin	32	N/A	No Connect
7	N/A	No Connect	33	SATA_RX+	SATA Differential RX+
8	N/A	No Connect	34	GND	System ground
9	GND	System ground	35	GND	System ground
10	N/A	No Connect	36	Reserved	Reserved pin
11	N/A	No Connect	37	GND	System ground
12	N/A	No Connect	38	Reserved	Reserved pin
13	N/A	No Connect	39	+3.3V	DC 3.3V input source

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Pin#	Assignment	Description	Pin#	Assignment	Description
14	N/A	No Connect	40	GND	System ground
15	GND	System ground	41	+3.3V	DC 3.3V input source
16	N/A	No Connect	42	N/A	No Connect
17	N/A	No Connect	43	N/A	No Connect
18	GND	System ground	44	N/A	No Connect
19	Reserved	Reserved pin	45	Reserved	No Connect
20	Reserved	Reserved pin	46	N/A	No Connect
21	GND	System ground	47	Reserved	No Connect
22	N/A	No Connect	48	Reserved	Reserved pin
23	SATA_TX+	SATA Differential TX+	49	GND	System ground
24	+3.3V	DC 3.3V input source	50	GND	System ground
25	SATA_TX-	SATA Differential TX-	51	GND	System ground
26	GND	System ground	52	+3.3V	DC 3.3V input source

[Table 3-1] Pin Assignments

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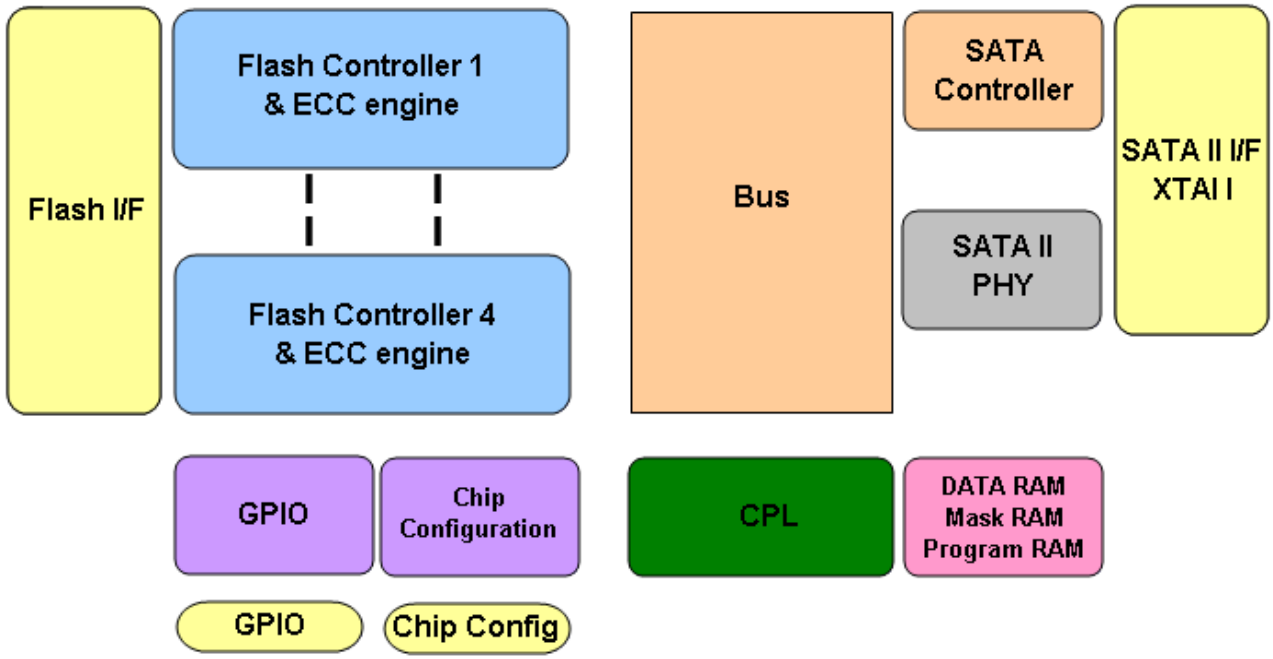
3.2 SSD Function Block Diagram

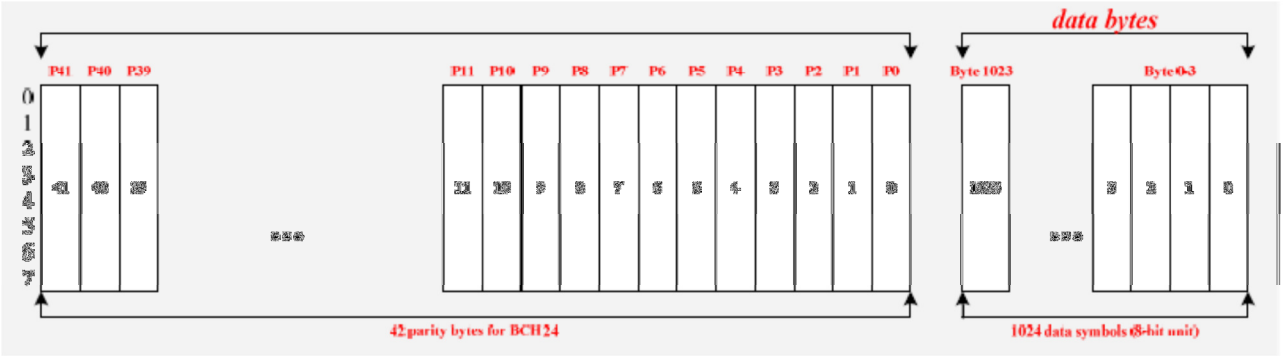


[Figure 3-2] Function Diagram

3.3 ECC Description

Please refer to FIG. 4 that is a diagram illustrating an allocating method of a spare area in each page of a NAND flash memory, where in the specific ECC algorithm utilizes a Bose, Chaudhuri and Hocquengham (BCH) ECC algorithm. When a BCH 16 ECC algorithm encodes the data in the NAND flash memory, the parity code generated in the encoding process may occupy 28 bytes of the spare area in each page. When a BCH 24 ECC algorithm encodes the data in the NAND flash memory, the parity code generated in the encoding process may occupy 42 bytes of the spare area in each page.

When a BCH 16 algorithm decodes the data in the NAND flash memory, the data can be decoded correctly if the error bit happened in two sector (1024Bytes) is 16. When a BCH 24 algorithm decodes the data in the NAND flash memory, the data can be decoded correctly if the error bit happened in two sector is 24.



[Figure 3-3] ECC Description

4.0 Product Specifications

4.1 System Interface and Configuration

• Burst read/write rate is 130 MB/sec (3.0 Gb/sec).
• Supports 1-port 1.5/3.0Gbps SATA I/II interface.
• Compliant with Serial ATA International Organization: Serial ATA Revision 2.6.
• Compliant SSD Allion compliance program.

4.2 System Performance

The ADATA SSD meets the performance requirements listed in below table.

The performance was measured on a computer system with following setup:

• Platform: ASUA P5K3 Deluxe (Intel P35 + ICH9)

• Operation Systems: Windows XP SP3

• Testing Utility: CrystalDiskMark v3.0

IXM26 (MLC)	Windows OS	
	Read (Minimum) / (Maximum)	Write (Minimum) / (Maximum)
4GB	30MB/s / 34MB/s	5MB/s / 5.8MB/s
.8GB	60MB/s / 66MB/s	10MB/s / 13MB/s
16GB	70MB/s / 75MB/s	15MB/s / 21MB/s
32GB	80MB/s / 84MB/s	35MB/s / 43MB/s

IXM26 (SLC)	Windows OS	
	Read (Minimum) / (Maximum)	Write (Minimum) / (Maximum)
1GB	60 MB/s / 70 MB/s	15MB/s / 22MB/s
2GB	70MB/s / 78MB/s	30MB/s / 36MB/s
4GB	70MB/s / 74MB/s	25MB/s / 30MB/s
8GB	75MB/s / 81MB/s	35MB/s / 42MB/s
16GB	80MB/s / 86MB/s	75MB/s / 81MB/s
32GB	80MB/s / 87MB/s	80MB/s / 85MB/s

Actual performance may vary depending on use conditions and environment

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4.3 Drive Capacity

Capacity	Cylinders	Heads	Sectors	Max LBA
1GB	1,959	16	63	1,974,672
2GB	3,897	16	63	3,928,176
4GB	7,773	16	63	7,835,184
8GB	16,383	16	63	15,649,200
16GB	16,383	16	63	31,277,232
32GB	16,383	16	63	62,533,296

4.4 Supply Voltage

Item	Requirements
Allowable voltage	3.3V ± 5%
Allowable noise/ripple	100mV p-p or less

4.5 System Power Consumption

Power	Max
Active	<2W
Idle/Standby/Sleep	< 0.7W

4.6 System Reliability

MTBF	>1,000,000 Hours

4.7 Environmental Specifications

Feature	Commercial	industrial
Temperature	0℃ to 70℃	-40℃ to 85℃

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Humidity	0℃ to 55℃ / 5%~95% RH, non-condensing
Vibration	20G Peak, 80~2000Hz
Shock	1500G, duration 0.5ms, Half Sine Wave

*Note: Depends on Flash memory specifications.

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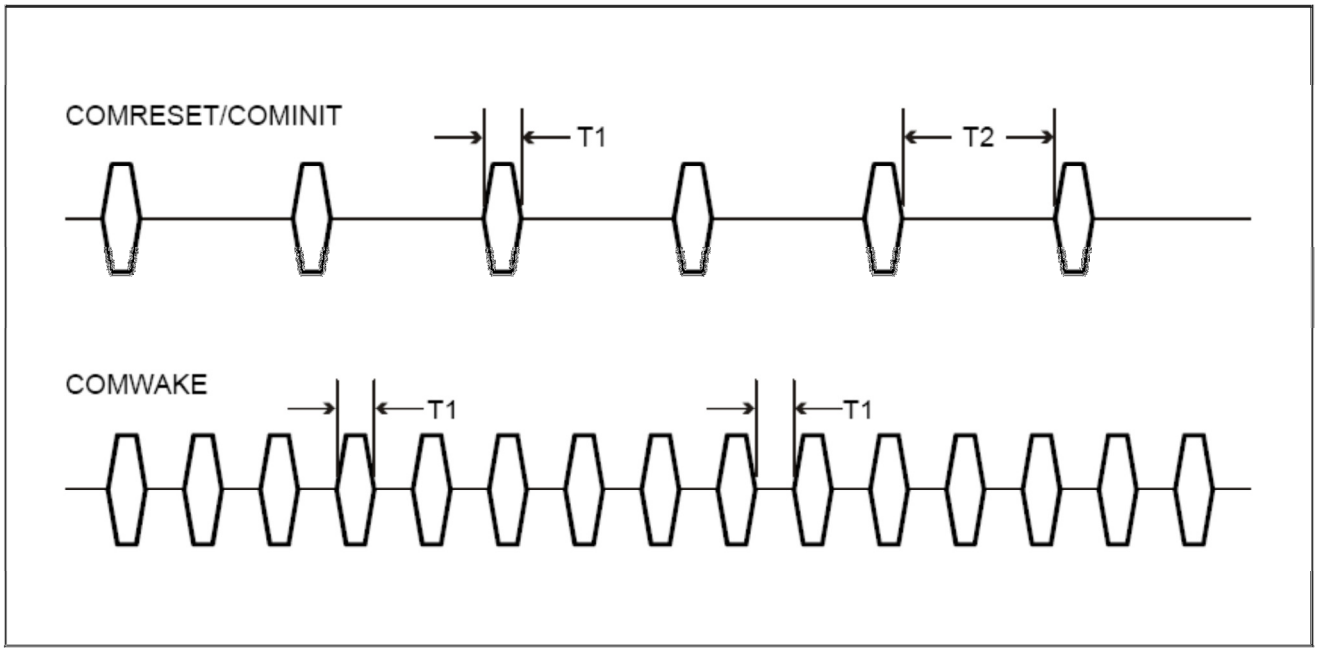
5.0 SATA Interface

5.1 Out of bank signaling

The shall be tree Out Of Band (OOB) signals used/ detected by the Phy: COMRESET, COMINIT, and COMWAKE. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in following Figure and Table. The COMWAKE OOB signaling is used to bring the Phy out of a power-down state (Partial or Slumber).

There shall be three Out Of Band (OOB) signals used/detected by the Phy: COMRESET, COMINIT, and COMWAKE. COMINIT, COMRESET and COMWAKE OOB signaling shall be achieved by transmission of either a burst of four Gen1 ALIGNP primitives or a burst composed of four Gen1 Dwords with each Dword composed of four D24.3 characters, each burst having duration of 160 UIOOB. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in Figure 6-1 and Table 6-1.



[Figure 5-1] OOB signals

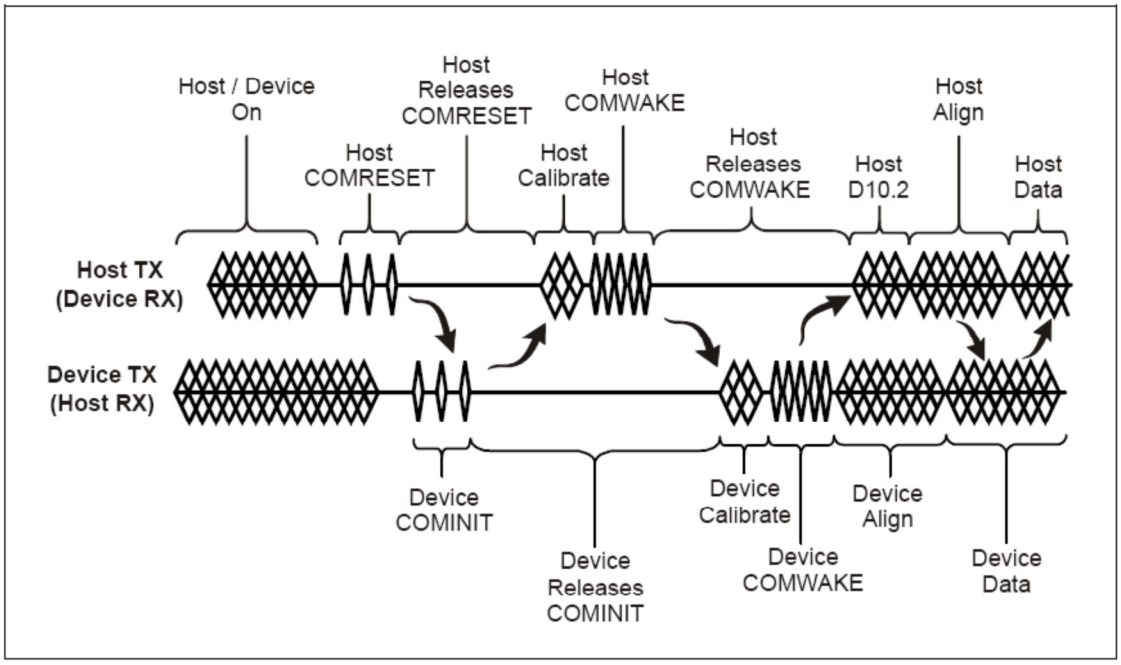
Time	Value
T1	160 UIoob (106.7 ns nominal)
T2	480 UIoob (320 ns nominal)

[Table 5-1] OOB Signal Times

5.2 COMRESET sequence state diagram

COMRESET always originates from the host controller, and forces a hardware reset in the device. It is indicated by transmitting bursts of data separated by an idle bus condition. The OOB COMRESET signal shall consist of no less than six data bursts, including inter-burst temporal spacing. The COMRESET signal shall be:
1) Sustained/continued uninterrupted as long as the system hard reset is asserted, or 2) Started during the system hardware reset and ended some time after the negation of system hardware reset, or 3) Transmitted immediately following the negation of the system hardware reset signal.

The host controller shall ignore any signal received from the device from the assertion of the hardware reset signal until the COMRESET signal is transmitted. Each burst shall be 160 Gen1 UI's long (106.7 ns) and each inter-burst idle state shall be 480 Gen1 UI's long (320 ns). A COMRESET detector looks for four consecutive bursts with 320 ns spacing (nominal). Any spacing less than 175 ns or greater than 525 ns shall invalidate the COMRESET detector output. The COMRESET interface signal to the PHY layer shall initiate the Reset sequence shown in Figure 6-2 below. The interface shall be held inactive for at least 525 ns after the last burst to ensure far-end detector detects the negation properly.



[Figure 5-2] COMRESET Sequence

Description:

1. Host/device are powered and operating normally with some form of active communication.
2. Some condition in the host causes the host to issue COMRESET
3. Host releases COMRESET. Once the condition causing the COMRESET is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
4. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
5. Host calibrates and issues a COMWAKE.
6. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.
7. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters (see 7.6) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.
8. Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.
9. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is

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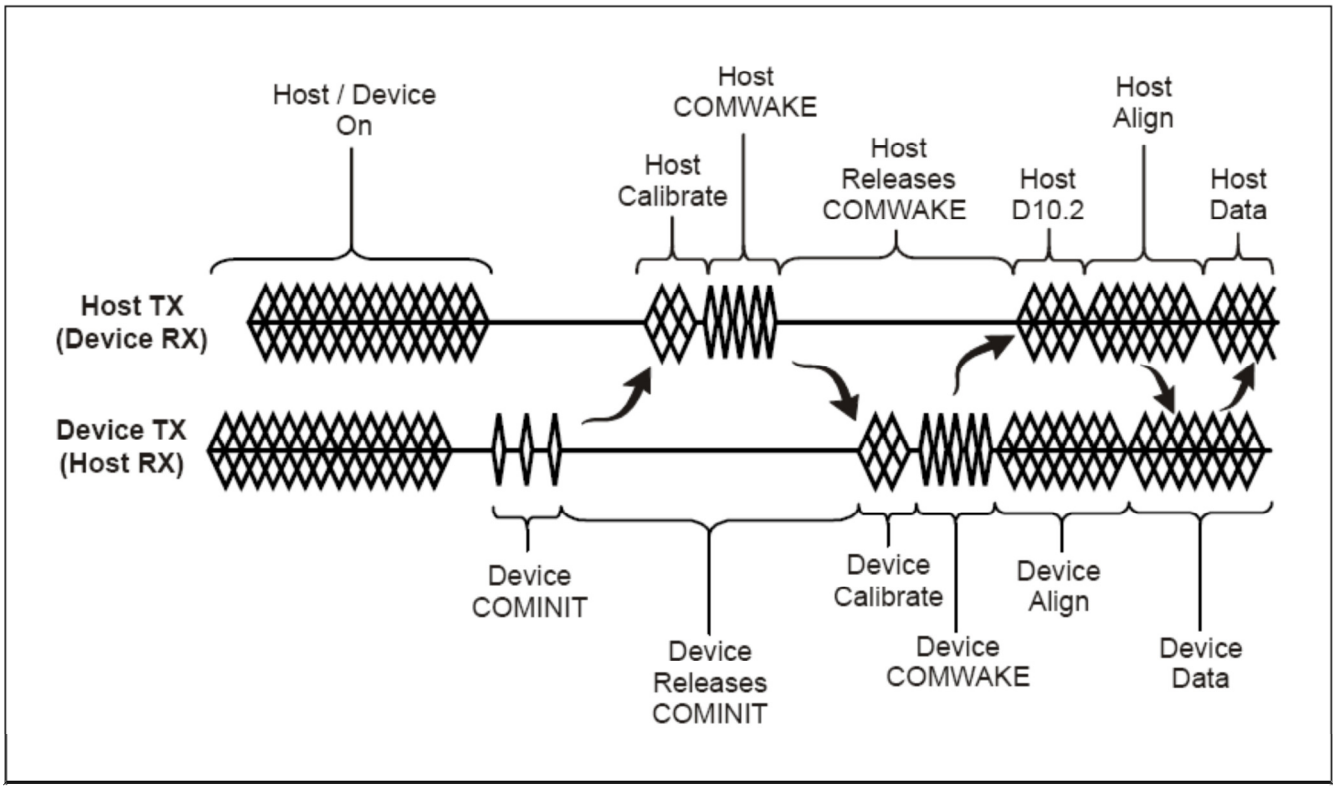
established and normal operation may begin.

5.3 COMINIT

COMINIT always originates from the drive and requests a communication initialization. It is electrically identical to the COMRESET signal except that it originates from the device and is sent to the host. It is used by the device to request a reset from the host in accordance to the sequence shown in Figure 6-3, below.



[Figure 5-3] COMINIT Sequence

Description:

1. Host/device are powered and operating normally with some form of active communication.
2. Some condition in the device causes the device to issues a COMINIT
3. Host calibrates and issues a COMWAKE.
4. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent

for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.

5. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters (see section 7.6) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6 us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.
6. Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.
7. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

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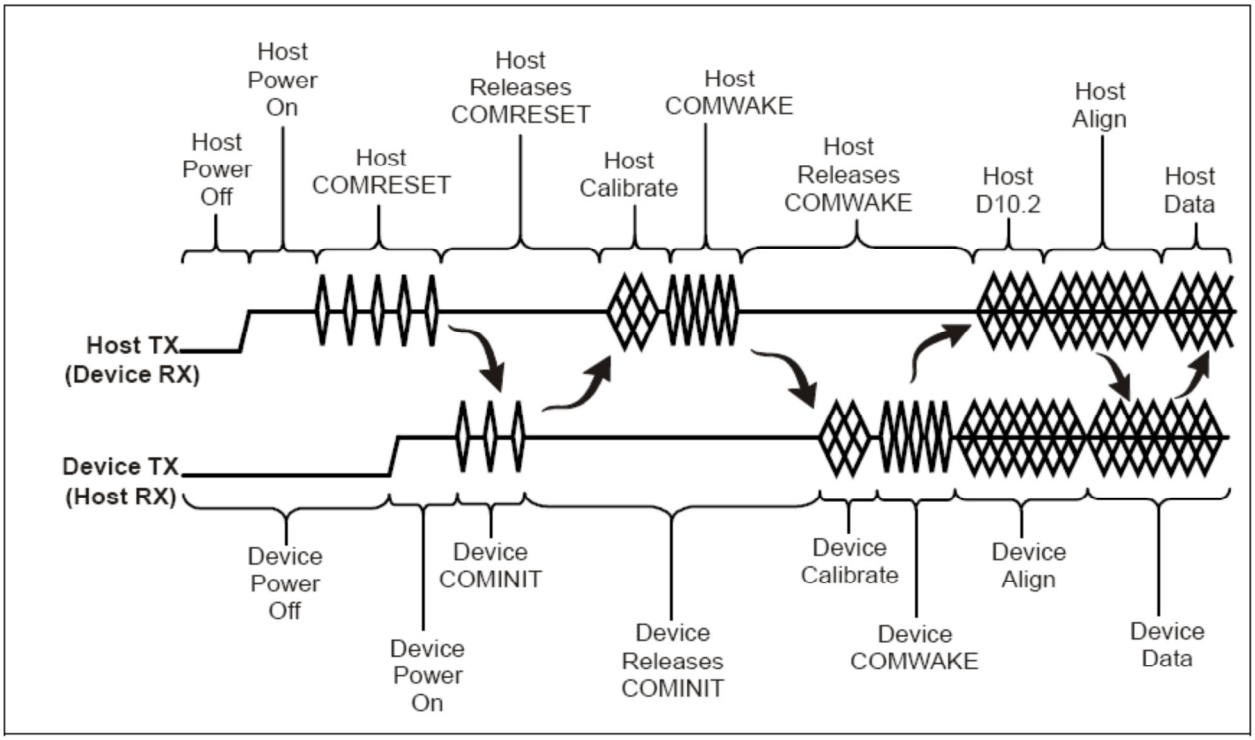
5.4 Power on sequence timing diagram

The following timing diagrams and descriptions are provided for clarity and are informative. The state diagrams provided in section 8.4 comprise the normative behavior specification and is the ultimate reference.



[Figure 5-4] Power on sequence

Description:

1. Host/device power-off - Host and device power-off.
2. Power is applied - Host side signal conditioning pulls TX and RX pairs to neutral state (common mode voltage).
3. Host issues COMRESET
4. Host releases COMRESET. Once the power-on reset is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
5. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
6. Host calibrates and issues a COMWAKE.
7. Device responds – The device detects the COMWAKE sequence on its RX pair and

calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP primitives have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP primitives at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device shall enter an error state.

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9. Device locks – the device locks to the ALIGN sequence and, when ready, sends the SYNCP primitive indicating it is ready to start normal operation.
10. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

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5.5 ATA Command Register

This table with the following paragraphs summarizes the ATA command set.

Command Table

Command Name	Code	PARAMETERS USED					
		SC	SN	CY	DR	HD	FT
CHECK POWER MODE	E5h	O	X	X	O	X	X
DEVICE CONFIGURATION OVERLAY	B1h	X	X	X	O	X	O
EXECUTE DIAGNOSTICS	90h	X	X	X	O	X	X
FLUSH CACHE	E7h	X	X	X	O	X	X
FLUSH CACHE EXT	EAh	X	X	X	O	X	X
IDENTIFY DEVICE	ECh	X	X	X	O	X	X
IDLE	E3h	O	X	X	O	X	X
IDLE IMMEDIATE	E1h	X	X	X	O	X	X
NOP	00h	F	F	F	O	X	O
INITIALIZE DEVICE PARAMETERS	91h	O	X	X	O	O	X
READ BUFFER	E4H	X	X	X	O	X	X
READ DMA	C8h or C9h	O	O	O	O	O	X
READ DMA EXT	25h	O	O	O	O	O	X
READ FPDMA QUEUED	60h	O	O	O	O	O	O
READ LOG EXT	2Fh	O	O	O	O	O	O
READ MULTIPLE	C4h	O	O	O	O	O	X
READ MULTIPLE EXT	29h	O	O	O	O	O	X
READ NATIVE MAX ADDRESS	F8h	X	X	X	O	X	X
READ NATIVE MAX ADDRESS EXT	27h	X	X	X	O	X	X
READ SECTOR(S)	20h or 21h	O	O	O	O	O	X
READ SECTOR(S) EXT	24h	O	O	O	O	O	X
READ VERIFY SECTOR(S)	40h or 41h	O	O	O	O	O	X
READ VERIFY SECTOR(S) EXT	42h	O	O	O	O	O	X
RECALIBRATE	10h	X	X	X	O	X	X
SECURITY DISABLE PASSWORD	F6h	X	X	X	O	X	X
SECURITY ERASE PREPARE	F3h	X	X	X	O	X	X
SECURITY ERASE UNIT	F4h	X	X	X	O	X	X

SECURITY FREEZE LOCK	F5h	X	X	X	O	X	X
SECURITY SET PASSWORD	F1h	X	X	X	O	X	X
SECURITY UNLOCK	F2h	X	X	X	O	X	X
SEEK	7xh	X	X	O	O	O	X
SET FEATURES	EFh	O	X	X	O	X	O
SET MAX	F9h	O	O	O	O	O	O
SET MAX ADDRESS EXT	37h	O	O	O	O	O	X
SET MULTIPLE MODE	C6h	O	X	X	O	X	X
SLEEP	E6h	X	X	X	O	X	X
SMART	B0h	X	X	O	O	X	O
STANDBY	E2h	X	X	X	O	X	X
STANDBY IMMEDIATE	E0h	X	X	X	O	X	X
WRITE BUFFER	E8h	X	X	X	O	X	X
WRITE DMA	CAh or CBh	O	O	O	O	O	X
WRITE DMA EXT	35h	O	O	O	O	O	X
WRITE DMA FUA EXT	3Dh	O	O	O	O	O	X
WRITE FPDMA QUEUED	61h	O	O	O	O	O	O
WRITE LOG EXT	3Fh	O	O	O	O	O	X
WRITE MULTIPLE	C5h	O	O	O	O	O	X
WRITE MULTIPLE EXT	39h	O	O	O	O	O	X
WRITE MULTIPLE FUA EXT	CEh	O	O	O	O	O	X
WRITE SECTOR(S)	30h or 31h	O	O	O	O	O	X
WRITE SECTOR(S) EXT	34h	O	O	O	O	O	X
WRITE VERIFY	3Ch	O	O	O	O	O	O

Note:

O = Valid, X = Don't care

SC = Sector Count Register

SN = Sector Number Register

CY = Cylinder Low/High Register

DR = DEVICE SELECT Bit (DEVICE/HEAD Register Bit 4)

HD = HEAD SELECT Bit (DEVICE/HEAD Register Bit 3-0)

FT = Features Register

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5.6 ATA COMMAND SPECIFICATIONS

CHECK POWER MODE (E5h)

The host can use this command to determine the current power management mode.
Sector Count result value-

00h – device is in Standby mode
80h – device is in Idle mode
FFh – device is in Active mode or Idle mode

DEVICE CONFIGURATION OVERLAY (B1h)

Individual Device Configuration Overlay (DCO) feature set commands are identified by the value placed in the Feature field.The subcommands and their respective codes are listed below.

Device Configuration Overlay Feature field values

Value	Commands
C0h	DEVICE CONFIGURATION RESTORE
C1h	DEVICE CONFIGURATION FREEZE LOCK
C2h	DEVICE CONFIGURATION IDENTIFY
C3h	DEVICE CONFIGURATION SET

DEVICE CONFIGURATION RESTORE (B1h/C0h)

The DEVICE CONFIGURATION RESTORE command provides a method for a host to restore any setting previously changed by a DEVICE CONFIGURATION SET command and to restore the content of the IDENTIFY DEVICE data, IDENTIFY PACKET DEVICE data, and other feature settings in a device to their factory default settings. The results of this action are indicated by the data returned from the Input Data of a DEVICE CONFIGURATION IDENTIFY command.

DEVICE CONFIGURATION FREEZE LOCK (B1h/C1h)

The DEVICE CONFIGURATION FREEZE LOCK command provides a method for the host to prevent accidental modification of a device's DCO settings. After a device has completed a DEVICE CONFIGURATION FREEZE LOCK command without error, the device shall return command aborted for all DEVICE CONFIGURATION SET, DEVICE

CONFIGURATION FREEZE LOCK, DEVICE CONFIGURATION IDENTIFY, and DEVICE CONFIGURATION RESTORE commands until after the device processes a power-on reset. A device shall be in the factory_config state or the reduced_config state after processing a power-on reset. A device shall not exit the DCO_Locked state as the result of processing a hardware reset or a software reset.

DEVICE CONFIGURATION IDENTIFY (B1h/C2h)

The DEVICE CONFIGURATION IDENTIFY command causes a device to return a 512-byte data structure. The content of this data structure indicates the selectable commands, modes, and feature sets that the device is capable of disabling or modifying through processing of a DEVICE CONFIGURATION SET command. If a DEVICE CONFIGURATION SET command reducing a device's capabilities has completed without error, then:

a) the response by a device to an IDENTIFY DEVICE, IDENTIFY PACKET DEVICE, and other commands, except the DEVICE CONFIGURATION IDENTIFY command, shall reflect the reduced set of capabilities; and
b) the response by a device to a DEVICE CONFIGURATION IDENTIFY command shall reflect the entire set of selectable capabilities.

The phrase “is changeable” indicates that the feature may be disabled by the host using a DEVICE CONFIGURATION SET command. If the feature is not changeable then the device may support the feature but the DEVICE CONFIGURATION SET command shall not affect support of the feature.

The format of the Device Configuration Overlay data structure is listed below.

DCO Identify data structure

Word	Value	Description
0	0002h	Data structure revision number
1	0007h	Multiword DMA modes supported Bit15:3 Reserved Bit2 1 = Reporting support for Multiword DMA mode 2 and below is changeable Bit1 1 = Reporting support for Multiword DMA mode 1 and below is changeable Bit0 1 = Reporting support for Multiword DMA mode 0 is changeable
2	007Fh	Ultra DMA modes supported Bit15:7 Reserved Bit6 1 = Reporting support for Ultra DMA mode 6 and below is changeable Bit5 1 = Reporting support for Ultra DMA mode 5 and below is changeable Bit4 1 = Reporting support for Ultra DMA mode 4 and below is changeable Bit3 1 = Reporting support for Ultra DMA mode 3 and below is changeable Bit2 1 = Reporting support for Ultra DMA mode 2 and below is changeable Bit1 1 = Reporting support for Ultra DMA mode 1 and below is changeable Bit0 1 = Reporting support for Ultra DMA mode 0 is changeable
3-6	Native MAX LBA	Maximum LBA (QWord) Bit63:48 Reserved Bit47:0 Maximum LBA
7	0089h	Command set/feature set supported part 1 Bit15 Reserved Bit14 1 = Reporting support for the Write-Read-Verify feature set is changeable Bit13 1 = Reporting support for the SMART Conveyance self-test is changeable Bit12 1 = Reporting support for the SMART Selective self-test is changeable Bit11 1 = Reporting support for the Forced Unit Access is changeable Bit10 Reserved for TLC Bit9 1 = Reporting support for the Streaming feature set is changeable Bit8 1 = Reporting support for the 48-bit Addressing feature set is changeable Bit7 1 = Reporting support for the HPA feature set is changeable Bit6 1 = Reporting support for the AAM feature set is changeable Bit5 1 = Reporting support for the TCQ feature set is changeable

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		Bit4 1 = Reporting support for the PUIS feature set is changeable Bit3 1 = Reporting support for the Security feature set is changeable Bit2 1 = Reporting support for the SMART error log is changeable Bit1 1 = Reporting support for the SMART self-test is changeable Bit0 1 = Reporting support for the SMART feature set is changeable
8	0000h	Serial ATA Command set/feature set supported Bit15:5 Reserved for Serial ATA Bit4 1 = Reporting support for the SSP feature set is changeable Bit3 1 = Reporting support for asynchronous notification is changeable Bit2 1 = Reporting support for interface power management is changeable Bit1 1 = Reporting support for non-zero buffer offsets is changeable Bit0 1 = Reporting support for the NCQ feature set is changeable
9	0000h	Reserved for Serial ATA
10-20	0000h	Reserved
21	0000h	Command set/feature set supported part 2 Bit15 1 = Reporting support for the NV Cache feature set is changeable Bit14 1 = Reporting support for the NV Cache Power Management feature set is changeable Bit13 1 = Reporting support for WRITE UNCORRECTABLE EXT is changeable Bit12 1 = Reporting support for the Trusted Computing feature set is changeable Bit11 1 = Reporting support for the Free-fall Control feature set is changeable Bit10:0 Reserved
22	0000h	Command set/feature set supported part 3 Bit15:0 Reserved
23-207	0000h	Reserved
208-254	0000h	Vender Specific
255	Checksum + A5h	Integrity word Bit15:8 Checksum Bit7:0 Signature

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DEVICE CONFIGURATION SET (B1h/C3h)

The DEVICE CONFIGURATION SET command allows a host to reduce the set of optional commands, modes, or feature sets supported by a device as indicated by a DEVICE CONFIGURATION IDENTIFY command. The DEVICE CONFIGURATION SET command may modify the data returned by IDENTIFY DEVICE or IDENTIFY PACKET DEVICE. When the IDENTIFY DEVICE data or IDENTIFY PACKET DEVICE data is changed, the device shall respond in a manner consistent with the new data.

If a bit is set to one in the DEVICE CONFIGURATION SET data transmitted to the device that is not set in the DCO data received from a DEVICE CONFIGURATION IDENTIFY command, no action is taken for that bit.

Modifying the maximum LBA of the device also modifies the LBA value returned by a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command.

EXECUTE DIAGNOSITICS (90h)

This command performs the internal diagnostic tests implemented by the drive. See ERROR register for diagnostic codes.

FLUSH CACHE (E7h)

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

FLUSH CACHE EXT (EAh)

48-bit feature set mandatory command. This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

IDENTIFY DEVICE (ECh)

This commands read out 512Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

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Identify Device Information Default Value

Word	Value	F/V	Description
0	0040h		General configuration
		F	15 0 = ATA device
		X	14-8 Retired
		X	7-6 Obsolete
		X	5-3 Retired
		V	2 Response incomplete
		X	1 Retired
			0 Reserved
1	3FFFh	F	Number of logical cylinders
2	C837h	V	Specific configuration
3	0010h	F	Number of logical heads
4-5	0000h	X	Retired
6	003Fh	F	Number of logical sector per logical track
7-8	0000h		Reserved for assignment by the CompactFlash_ Association
9	0000h	X	Retired
10-19	XXXXh	F	Serial number (20 ASCII characters)
20-21	0000h	X	Retired
22	0000h	X	Obsolete
23-26	XXXXh	F	Firmware revision (8 ASCII characters)
27-46	XXXXh	F	Model number (40 ASCII characters)
47	8001h	F	15-8 80h
		F	7-0 00h = Reserved
		F	01h = Maximum number of 1 sectors on READ/WRITE MULTIPLE commands
48	0000h	F	Reserved
49	2F00h		Capabilities
			15-14 Reserved for the IDENTIFY PACKET DEVICE command.
		F	13 1 = Standby timer values as specified in this standard are supported
			0 = Standby timer values shall be managed by the device
		F	12 Reserved for the IDENTIFY PACKET DEVICE command.

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			11 1 = IORDY supported
		F	0 = IORDY may be supported
		F	10 1 = IORDY may be disabled
		F	9 1 = LBA supported
		X	8 1 = DMA supported.
			7-0 Retired
50	4000h		Capabilities
		F	15 Shall be cleared to zero.
		F	14 Shall be set to one.
			13-2 Reserved.
		X	1 Obsolete
		F	0 Shall be set to one to indicate a device specific Standby timer value minimum.
51	0000h	F	15-8 PIO data transfer cycle timing mode
			7-0 Reserved
52	0000h	X	Obsolete
53	0007h	F	15-3 Reserved
		F	2 1 = the fields reported in word 88 are valid
			0 = the fields reported in word 88 are not valid
		F	1 1 = the fields reported in words 70:64 are valid
			0 = the fields reported in words 70:64 are not valid
		X	0 1 = the fields reported in words 58:54 are valid
			0 = the fields reported in words 58:54 are not valid
54	XXXXh	X	Number of current cylinders
55	00XXh	X	Number of current heads
56	XXXXh	X	Number of current sector per track
57-58	XXXXh	X	Current capacity in sectors
59	0101h		15-9 Reserved
		V	8 1 = Multiple sector setting is valid
		V	7-0 xxh = Setting for number of sectors that shall be transferred per interrupt on R/W Multiple command
60-61	XXXXh	F	Total number of user addressable sectors
62	0000h	X	Obsolete

63	0007h	F V V V F F F	15-11 Reserved 10 1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected 9 1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected 8 1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected 7-3 Reserved 2 1 = Multiword DMA mode 2 and below are supported 1 1 = Multiword DMA mode 1 and below are supported 0 1 = Multiword DMA mode 0 is supported
64	0003h	 F	15-8 Reserved 7-0 Advanced PIO modes supported
65	0078h	F	Minimum Multiword DMA transfer cycle time per word
66	0078h	F	Manufacturer's recommended Multiword DMA transfer cycle time
67	0078h	F	Minimum PIO transfer cycle time without flow control
68	0078h	F	Minimum PIO transfer cycle time with IORDY flow control
69-70	0000h		Reserved
71-74	0000h		Reserved for the IDENTIFY PACKET DEVICE command
75	0000h	 F	Queue depth 15-5 Reserved 4-0 Maximum queue depth – 1
76	0206h	 F F F F F F	Serial ATA Capabilities 15-11 Reserved for Serial ATA 10 1 = Supports PHY Event Counts 9 1 = Supports receipt of host initiated power management requests 8 1 = Supports the NCQ feature set 7-3 Reserved for Serial ATA 2 1 = Supports SATA Gen2 Signaling Speed (3.0Gb/s) 1 1 = Supports SATA Gen1 Signaling Speed (1.5Gb/s) 0 Shall be cleared to zero
77	0000h		Reserved for Serial ATA

78	0008h		Serial ATA feature supported
			15-7 Reserved for Serial ATA
		F	6 1 = Device supports Software Settings Preservation
			5 Reserved for Serial ATA
		F	4 1 = Device supports in-order data delivery
		F	3 1 = Device supports initiating power management
		F	2 1 = Device supports DMA Setup auto-activation
		F	1 1 = Device supports non-zero buffer offsets
		F	0 Shall be cleared to zero
79	0000h		Serial ATA feature enabled
			15-7 Reserved for Serial ATA
		V	6 1 = Software Settings Preservation enabled
			5 Reserved for Serial ATA
		V	4 1 = In-order data delivery enabled
		V	3 1 = Device initiated power management enabled
		V	2 1 = DMA Setup auto-activation enabled
		V	1 1 = Non-zero buffer offsets enabled
		F	0 Shall be cleared to zero
80	00F0h		Major version number 0000h or FFFFh = device does not report version
			15 Reserved
		F	14 Reserved for ATA/ATAPI-14
		F	13 Reserved for ATA/ATAPI-13
		F	12 Reserved for ATA/ATAPI-12
		F	11 Reserved for ATA/ATAPI-11
		F	10 Reserved for ATA/ATAPI-10
		F	9 Reserved for ATA/ATAPI-9
		F	8 Reserved for ATA/ATAPI-8
		F	7 1 = supports ATA/ATAPI-7
		F	6 1 = supports ATA/ATAPI-6
		F	5 1 = supports ATA/ATAPI-5
		F	4 1 = supports ATA/ATAPI-4
		F	3 Obsolete
		X	2 Obsolete

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		X	1 Obsolete
			0 Reserved
81	0000h	F	Minor version number
82	302Bh		Command and feature sets supported
		X	15 Obsolete
		F	14 1 = NOP command supported
		F	13 1 = READ BUFFER command supported
		F	12 1 = WRITE BUFFER command supported
		X	11 Obsolete
		F	10 1 = Host Protected Area feature set supported
		F	9 1 = DEVICE RESET command supported
		F	8 1 = SERVICE interrupt supported
		F	7 1 = release interrupt supported
		F	6 1 = look-ahead supported
		F	5 1 = write cache supported
		F	4 Shall be cleared to zero to indicate that the PACKET Command
		F	feature set is not supported.
		F	3 1 = mandatory Power Management feature set supported
		F	2 1 = Removable Media feature set supported
		F	1 1 = Security Mode feature set supported
			0 1 = SMART feature set supported
83	5000h		Command and feature sets supported
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13 1 = The FLUSH CACHE EXT command is supported
		F	12 Shall be set to one to indicate that the mandatory FLUSH CACHE
		F	command is supported
		F	11 1 = The DCO feature set is supported
		F	10 1 = The 48-bit Address feature set is supported
		F	9 1 = The AAM feature set is supported
			8 1 = SET MAX security extension supported
		F	7 Reserved
		F	6 1 = SET FEATURES subcommand required to spin up after

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		F	power-up
		F	5 1 = Power-Up In Standby feature set supported
		F	4 1 = Removable Media Status Notification feature set supported
		F	3 1 = Advanced Power Management feature set supported
		F	2 1 = CFA feature set supported
			1 1 = READ/WRITE DMA QUEUED supported
			0 1 = DOWNLOAD MICROCODE command supported
84	4000h		Command and feature sets supported
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13 1 = The IDLE IMMEDIATE command with UNLOAD feature is supported
		X	12-11 Reserved for TLC
		F	10-9 Obsolete
		F	8 1 = The 64-bit World wide name is supported
		F	7 1 = The WRITE DMA QUEUED FUA EXT command is supported
		F	6 1 = The WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported
		F	5 1 = The GPL feature set is supported
		F	4 1 = The Streaming feature set is supported
		F	3 1 = The Media Card Pass Through Command feature set is supported
			2 1 = Media serial number is supported
			1 1 = SMART self-test supported
			0 1 = SMART error logging supported
85	3029h		Command and feature sets supported or enable
		X	15 Obsolete
		F	14 1 = The NOP command is supported
		F	13 1 = The READ BUFFER command is supported
		F	12 1 = The WRITE BUFFER command is supported
		X	11 Obsolete
		V	10 1 = HPA feature set is supported
		F	9 Shall be cleared to zero to indicate that the DEVICE RESET

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		V	command is not supported
		V	8 1 = The SERVICE interrupt is enabled
		V	7 1 = The release interrupt is enabled
		V	6 1 = Read look-ahead is enabled
		F	5 1 = The volatile write cache is enabled
		F	4 Shall be cleared to zero to indicate that the PACKET Command
		X	feature set is not supported.
		V	3 Shall be set to one to indicate that the mandatory Power
		V	Management feature is supported
			2 Obsolete
			1 1 = The Security feature set is enabled
			0 1 = The SMART feature set is enabled
86	1000h		Command and feature sets supported or enable
		F	15 1 = Words 119-120 are valid
			14 Reserved
		F	13 1 = FLUSH CACHE EXT command supported
		F	12 1 = FLUSH CACHE command supported
		F	11 1 = The DCO feature set is supported
		F	10 1 = The 48-bit Address feature set is supported
		V	9 1 = The AAM feature set is enable
		V	8 1 = The SET MAX security extension is enabled by SET MAX
			SET PASSWORD
		F	7 Reserved for Address Offset Reserved Area Boot Method
		V	6 1 = SET FEATURES subcommand required to spin-up after
		X	power-up
		V	5 1 = The PUIS feature set is enabled
		F	4 Obsolete
		F	3 1 = The APM feature set is enabled
		F	2 1 = The CFA feature set is supported
			1 1 = The TCQ feature set is supported
			0 1 = The DOWNLOAD MICROCODE command is supported
87	4000h		Command and feature sets supported or enabled
		F	15 Shall be cleared to zero

		F	14 Shall be set to one
		F	13 1 = The IDLE IMMEDIATE command with UNLOAD feature is supported
		X	12-11 Reserved for TLC
		F	10-9 Obsolete
		F	8 1 = The 64-bit World wide name is supported
		F	7 1 = The WRITE DMA QUEUED FUA EXT command is supported
		F	6 1 = The WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT
		X	commands are supported
		V	5 1 = The GPL feature set is supported
		V	4 Obsolete
		F	3 1 = The Media Card Pass Through Command feature set is
		F	supported
			2 1 = Media serial number is supported
			1 1 = SMART self-test supported
			0 1 = SMART error logging supported
88	203Fh		Ultra DMA modes
			15 Reserved
		V	14 1 = Ultra DMA mode 6 is selected
			0 = Ultra DMA mode 6 is not selected
		V	13 1 = Ultra DMA mode 5 is selected
			0 = Ultra DMA mode 5 is not selected
		V	12 1 = Ultra DMA mode 4 is selected
			0 = Ultra DMA mode 4 is not selected
		V	11 1 = Ultra DMA mode 3 is selected
			0 = Ultra DMA mode 3 is not selected
		V	10 1 = Ultra DMA mode 2 is selected
			0 = Ultra DMA mode 2 is not selected
		V	9 1 = Ultra DMA mode 1 is selected
			0 = Ultra DMA mode 1 is not selected
		V	8 1 = Ultra DMA mode 0 is selected
			0 = Ultra DMA mode 0 is not selected
			7 Reserved

		F	6 1 = Ultra DMA mode 6 and below are supported
		F	5 1 = Ultra DMA mode 5 and below are supported
		F	4 1 = Ultra DMA mode 4 and below are supported
		F	3 1 = Ultra DMA mode 3 and below are supported
		F	2 1 = Ultra DMA mode 2 and below are supported
		F	1 1 = Ultra DMA mode 1 and below are supported
		F	0 1 = Ultra DMA mode 0 is supported
89	0001h	F	15-8 Reserved 7-0 Time required for Normal Erase mode SECURITY ERASE UNIT command
90	0001h	F	15-8 Reserved 7-0 Time required for Enhanced Erase mode SECURITY ERASE UNIT command
91	0000h	V	Current APM level value
92	FFFEh	V	Master Password Identifier
93	0000h	X	Hardware reset result
94	0000h	F V	Current AAM value 15-8 Vendor's recommended AAM value 7-0 Current AAM value
95-99	0000h		Reserved
100-103	XXXXh	X	Total Number of User Addressable Logical Sectors for 48-bit commands (QWord)
104-105	0000h		Reserved
106	4000h	 F F F F F	Physical sector size / logical sector size 15 Shall be cleared to zero 14 Shall be set to one 13 1 = Device has multiple logical sectors per physical sector 12 1 = Device Logical Sector longer than 256 Words 11-4 Reserved 3-0 2x logical sectors per physical sector
107-118	0000h		Reserved
119	4000h	 F	Commands and feature sets supported (Continued from words 84:82) 15 Shall be cleared to zero

		F F F F F 	14 Shall be set to one 13-6 Reserved 5 1= The Free-fall Control feature set is supported 4 1 = The DOWNLOAD MICROCODE command with mode 3 is supported 3 1 = The READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported 2 1 = The WRITE UNCORRECTABLE EXT command is supported 1 1 = The Write-Read-Verify feature set is supported 0 Reserved for DDT
120	4000h	 F F V F F F V 	Commands and feature sets supported or enabled (Continued from words 87:85) 15 Shall be cleared to zero 14 Shall be set to one 13-6 Reserved 5 1= The Free-fall Control feature set is enabled 4 1 = The DOWNLOAD MICROCODE command with mode 3 is supported 3 1 = The READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported 2 1 = The WRITE UNCORRECTABLE EXT command is supported 1 1 = The Write-Read-Verify feature set is enabled 0 Reserved for DDT
121-126	0000h		Reserved for expended supported and enabled settings
127	0000h	X	Obsolete
128	0021h	 F V F F V V V	Security status 15-9 Reserved 8 Security level 0 = High, 1 = Maximum 7-6 Reserved 5 1 = Enhanced security erase supported 4 1 = Security count expired 3 1 = Security frozen 2 1 = Security locked

		V F	1 1 = Security enabled 0 1 = Security supported
129-159	0000h	X	Vendor specific
160-216	0000h		Reserved
217	0001h	F	Nominal media rotation rate
218-254	0000h		Reserved
255	0000h	X	Integrity word 15-8 Checksum 7-0 Signature

Key:
F/V = Fixed/variable content
F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.
V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.
X = the content of the word may be fixed or variable.

IDLE (E3h)

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

IDLE IMMEDIATE (E1h)

This command causes the device to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

NOP (00h)

The subcommand determines the effect on TCQ (Not supported) commands.

INITIALIZE DEVICE PARAMETERS (91h)

This command enables the host to set the number of logical sectors per track and the number of logical heads minus 1, per logical cylinder for the current CHS translation mode.

If the capacity of the device is less than 16,514,064 sectors, a device shall support the CHS translation described in words 1, 3, and 6 of the IDENTIFY DEVICE information. Support of other CHS translations is optional.

If the host requests a CHS translation that is not supported by the device, the device shall return command aborted. The device shall also clear bit 0 of word 53 in the IDENTIFY DEVICE data to zero, and the content of words 54, 55, 56, and (58:57) may be zero until a supported translation is requested by the host.

If the requested CHS translation is not supported, the device shall fail all media access commands with an ID Not Found error until a valid CHS translation is established.

READ BUFFER (E4h)

The READ BUFFER command enables the host to read a 512-byte block of data. The READ BUFFER and WRITE BUFFER commands shall be synchronized such that sequential WRITE BUFFER and READ BUFFER commands access the same data.

The command prior to a READ BUFFER command should be a WRITE BUFFER command. If the READ BUFFER command is not preceded by a WRITE BUFFER command, the data returned by READ BUFFER may be indeterminate.

READ DMA (C8h)

Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 256 sectors.

READ DMA EXT (25h)

48-bit feature set mandatory command. Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 65536 sectors.

READ FPDMA QUEUED (60h)

NCQ feature set mandatory 48-bit command. This command requests that data to be transferred from the device to the host.

READ LOG EXT (2Fh)

General purpose logging feature set mandatory 48-bit command. This command returns the specified log to the host.

Log Address	Log Name	Feature Set	R/W
00h	Log directory	N/A	RO
10h	NCQ Command Error	NCQ	RO

READ MULTIPLE (C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ MULTIPLE EXT (29h)

48-bit feature set mandatory command. This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ NATIVE MAX ADDRESS (F8h)

This command returns the native max address. The native max address returned is the maximum LBA that is valid when using the SET MAX ADDRESS command.

If the 48-bit Address feature set is supported and the 48-bit native max address is greater than 268 435 455, the READ NATIVE MAX ADDRESS command shall return a maximum value of 268 435 454.

READ NATIVE MAX ADDRESS EXT (27h)

This command returns the native max address. The native max address returned is the maximum LBA that is valid when using the SET MAX ADDRESS EXT command.

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READ SECTOR(S) (20h/21h)

This command reads 1 to 256 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.

READ SECTOR(S) EXT (24h)

48-bit feature set mandatory command. This command reads 1 to 65536 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of zero requests 65536 sectors. The transfer beings specified in the Sector Number register.

READ VERIFY SECTOR(S) (40h/41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

READ VERIFY SECTOR(S) EXT (42h)

48-bit feature set mandatory command. This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

RECALIBRATE (10h)

The current drive performs no processing if it receives this command. It is supported for backward compatibility with previous devices.

SECURITY DISABLE PASSWORD (F6h)

Disables any previously set user password and cancels the lock. The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

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SECURITY ERASE PREPARE (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. This command prevents accidental loss of data on the drive.

SECURITY ERASE UNIT (F4h)

The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY FREEZE LOCK (F5h)

Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock result in the Aborted Command error:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

SECURITY SET PASSWORD (F1h)

This command set user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table.

SECURITY UNLOCK (F2h)

This command disable LOCKED MODE of the device. This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information.

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SEEK (7xh)

This command is effectively a NOP command to the device although it does perform a range check.

SET FEATURES (EFh)

This command set parameter to Features register and set drive's operation. For transfer mode, parameter is set to Sector Count register. This command is used by the host to establish or select certain features.

Features register Value and settable operating mode

Value	Function
02h	Enable volatile write cache
03h	Set transfer mode
05h	Enable the APM feature set
10h	Enable use of SATA feature
55h	Disable read look-ahead feature
66h	Disable reverting t power on defaults by soft reset
82h	Disable volatile write cache
85h	Disable the APM feature set
90h	Disable use of SATA feature
AAh	Enable read look-ahead feature
CCh	Enable reverting to power-on defaults

The specific SATA features are defined as below:

Sector Count Value	Description
01h	Non-Zero buffer offset in DMA Setup FIS (Not supported)
02h	DMA Setup FIS Auto-Active optimization
03h	Device-Initiated interface power state transitions
04h	Guaranteed In0Order Data delivery (Not supported)
05h	Asynchronous Notification (Not supported)
06h	Software Settings Preservation

SET MAX (F9h)

Individual SET MAX commands are identified by the value placed in the Feature field.

SET MAX Feature field values

Value	Function
00h	Obsolete
01h	SET MAX SET PASSWORD
02h	SET MAX LOCK
03h	SET MAX UNLOCK
04h	SET MAX FREEZE LOCK
05h	SET MAX SET PASSWORD DMA (Not supported)
06h	SET MAX UNLOCK DMA (Not supported)
07h-FFh	Reserved

SET MAX ADDRESS (F9h)

After successful command completion, all read and write access attempts to an LBA greater than the LBA specified by the successful SET MAX ADDRESS command shall be rejected with the ID Not Found bit set to one. IDENTIFY DEVICE data words 60..61 shall reflect the maximum LBA set with this command.

If the device successfully processes a SET MAX ADDRESS command with an LBA less than the native max without error, and the 48-bit Address feature set is supported, then the value placed in IDENTIFY DEVICE data words 100..103 shall be the same as the value placed in IDENTIFY DEVICE data words 60..61.

SET MAX SET PASSWORD (F9h/01h)

This command requests a transfer of a single 512-byte block of data from the host. The password is not retained by the device after the device has processed a power-on reset.

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SET MAX LOCK (F9h/02h)

The device is HPA Locked when it successfully processes a SET MAX LOCK comand. When the device has successfully processed the SET MAX LOCK command, the HPA Security Extensions unlock counter shall be set to a value of five. After this command is completed any other SET MAX commands except SET MAX UNLOCK and SET MAX FREEZE LOCK shall be command aborted. The device shall remain in this state until a power-on reset has been processed or command completion without error of a SET MAX UNLOCK or SET MAX FREEZE LOCK command.

SET MAX UNLOCK (F9h/03h)

This command requests a transfer of a single 512-byte block of data from the host. The password supplied in the data transferred shall be compared with the password set by the SET MAX SET PASSWORD command.

If the device is locked from HPA commands and the password compare fails, then the device shall return command aborted and decrement the HPA Security Extensions unlock counter. This counter shall be decremented for each password mismatch when SET MAX UNLOCK is issued and the device is locked from HPA commands. When this counter reaches zero in a device, then the device shall return command aborted for all subsequent SET MAX UNLOCK commands until after the device has processed a power-on reset.

If the device is HPA Locked, the HPA Security Extensions unlock counter is not zero, and the password compare matches, then the device is HPA Unlocked and all SET MAX commands shall be accepted.

SET MAX FREEZE LOCK (F9h/04h)

After successful command completion, any subsequent SET MAX commands shall return command aborted until a power-on reset has been processed by the device.
Commands disabled by SET MAX FREEZE LOCK are:

a) SET MAX ADDRESS
b) SET MAX SET PASSWORD
c) SET MAX LOCK
d) SET MAX UNLOCK
e) SET MAX ADDRESS EXT

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SET MAX ADDRESS EXT (37h)

After successful command completion, all read and write access attempts to an LBA greater than the LBA specified by the successful SET MAX ADDRESS EXT command shall be rejected with an ID Not Found error. A host should not issue more than one non-volatile SET MAX ADDRESS EXT command after a power-on or hardware reset. The contents of IDENTIFY DEVICE data and the maximum LBA shall not be changed if a SET MAX ADDRESS EXT command fails.

After a successful SET MAX ADDRESS EXT command using a new maximum LBA the content of all IDENTIFY DEVICE data words shall comply.

A successful READ NATIVE MAX EXT command should immediately precede SET MAX ADDRESS EXT. If the device receives a SET MAX ADDRESS EXT that is not immediately preceded by READ NATIVE MAX EXT, the device shall report command aborted.

SET MULTIPLE MODE (C6h)

This command establishes the number of logical sectors in the DRQ data block count for READ MULTIPLE, READ MULTIPLE EXT, WRITE MULTIPLE, and WRITE MULTIPLE EXT commands. The content of the Count field shall be less than or equal to the value in IDENTIFY DEVICE data word 47 bits (7:0). The host should set the content of the Count field to 1, 2, 4, 8, 16, 32, 64 or 128.

Devices shall support the DRQ data block size specified in the IDENTIFY DEVICE data word 47 bits (7:0), and may also support smaller values.

Upon receipt of the command, the device checks the Count field. If the content of the Count field is not zero, the Count field contains a valid value, and the DRQ data block count is supported, then the value in the Count field is used for all subsequent READ MULTIPLE, READ MULTIPLE EXT, WRITE MULTIPLE, WRITE MULTIPLE EXT and WRITE MULTIPLE FUA EXT commands and their execution is enabled.

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If the content of the Count field is zero and the SET MULTIPLE command completes without error, then the device shall respond to any subsequent READ MULTIPLE, READ MULTIPLE EXT, WRITE MULTIPLE, WRITE MULTIPLE EXT, and WRITE MULTIPLE FUA EXT command with command aborted until a subsequent successful SET MULTIPLE command completion where the Count field is not set to zero. If the content of the Count field is zero, then the device may:

a) disable multiple mode (i.e.,respond with command aborted for all subsequent READ MULTIPLE, READ MULTIPLE EXT, WRITE MULTIPLE, WRITE MULTIPLE EXT, and WRITE MULTIPLE FUA EXT commands)
b) return command aborted for all SET MULTIPLE MODE commands; or
c) retain the previous multiple mode settings.

After a successful SET MULTIPLE command the device shall report the valid value set by that command in IDENTIFY DEVICE data word 59.

After a power-on or hardware reset, if IDENTIFY DEVICE data word 59 bit 8 is set to one and IDENTIFY DEVICE data word 59 bits (7:0) are cleared to zero, a SET MULTIPLE command is required before issuing a READ MULTIPLE, READ MULTIPLE EXT, WRITE MULTIPLE, or WRITE MULTIPLE EXT command. If bit 8 is set to one and bits (7:0) are not cleared to zero, a SET MULTIPLE command may be issued to change the multiple value required before issuing a READ MULTIPLE, READ MULTIPLE EXT, WRITE MULTIPLE, or WRITE MULTIPLE EXT command.

SLEEP (E6h)

This command is the only way to cause the device to enter Sleep mode. The device shall exit Sleep (i.e., State PM3) only after processing a hardware reset, a software reset, or a DEVICE RESET command. A device shall not power-on in Sleep mode.

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SMART Function Set (B0h)

Performs different processing required for predicting device failures, according to the subcommand specified in the Features register. If the Features register contains an unsupported value, the Aborted Command error is returned. If the SMART function is disabled, any subcommand other than SMART ENABLE OPERATIONS results in the Aborted Command error.

Code	Smart Subcommand
D0h	READ DATA
D1h	READ ATTRIBUTE THRESHOLDS
D2h	ENABLE/DISABLE ATTRIBUTE AUTOSAVE
D3h	SAVE ATTRIBUTE VALUES
D8h	ENABLE OPERATIONS
D9h	DISABLE OPERATIONS
DAh	RETURN STATUS

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SMART READ DATA (B0h/D0h)

This command returns 512-byte SMART Data Structure to the host with PIO data-in protocol. The register file has to contain D0h for Features register, 4Fh for LBA Mid register and C2h for the LBA High register.

Byte	Description
0-1	Data structure revision number
2-13	1st attribute data
14-361	2nd-30th Individual attribute data
362	Off-line data collection status
363	Self-test execution status
364-365	Total time in seconds to complete off-line data collection
366	Reserved
367	Off-line data collection capability
368-369	SMART capability
370	Error logging capability
371	Self-test Failure Checkpoint
372	Short self-test routine recommended polling time(in minutes)
373	Extended self-test routine recommended polling time(in minutes)
374-510	Reserved
511	Data structure Checksum

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Byte 2-361: Individual attributes data

Byte	Description
0	Attribute ID
1-2	Status Flag
3	Attribute Value (0x64)
4	Worst Ever normalized Attribute Value
5-10	Raw Attribute Value
11	Reserved

The attribute ID information is listed in the following table

ID	Description
01h	Read Error Rate
02h	Throughput Performance
03h	Spin Up Time
05h	Reallocated Sector Count
07h	Seek Error Rate
08h	Seek Time performance
09h	Power-On hours Count
0Ah	Spin Retry Count
0Ch	Drive Power Cycle Count
A8h	SATA PHY Error Count
AAh	Bad Block Count
ADh	Erase Count
AFh	Bad Cluster Table Count
C0h	Unexpected Power Loss Count
C2h	Temperature
C5h	Current Pending Sector Count
F0h	Write Head

SMART READ ATTRIBUTE THRESHOLD (B0h/D1h)

This transfers 512 bytes of drive failure threshold data to the host.

Byte	Description
0-1	Data structure revision number
2-361	1st – 30th Individual attribute threshold data
362-510	Reserved
511	Data structure checksum

SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE (B0h/D2h)

This command enables and disables the optional attribute autosave feature of the device. This command may either allow the device, after some vendor specified event, to save the device updated attributes to non-volatile memory; or this command may cause the autosave feature to be disabled. The state of the attribute autosave feature, either enabled or disabled, shall be preserved by the device during all power and reset events.

A value of zero written by the host into the device's Count field before issuing this command shall cause this feature to be disabled. Disabling this feature does not preclude the device from saving SMART data to non-volatile memory during some other normal operation (e.g., during a power-on or power-off sequence or during an error recovery sequence).

A value of F1h written by the host into the device's Count field before issuing this command shall cause this feature to be enabled. Any other other non-zero value written by the host into this field before issuing this command is vendor specific. The meaning of any non-zero value written to this field at this time shall be preserved by the device during all power and reset events.

SMART SAVE ATTRIBUTE VALUE (B0h/D3h)

Saves any modified attribute values.

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SMART ENABL OPERATIONS (B0h/D8h)

Enable the SMART function. This setting is maintained when the power is turned off and then back on. Once the SMART function is enabled, subsequent SMART ENABLE OPERATIONS commands do not affect any parameters.

SMART DISABLE OPERATIONS (B0h/D9h)

Disable the SMART function. Upon receiving the command, the drive disables all SMART operations. This setting is maintained when the power is turned off and then back on. Once this command has been received, all SMART commands other than SMART ENABLE OPERATIONS are aborted with the Aborted Command error.

This command disables all SMART capabilities including any and all timer and event count functions related exclusively to this feature. After command acceptance, this controller will disable all SMART operations. SMART data in no longer be monitored or saved. The state of SMART is preserved across power cycles.

SMART RETURN STATUS (B0h/DAh)

Report the drive reliability status.

Values reported when a predicted defect has not been detected:

Cylinder Low register: 4Fh

Cylinder High register: C2h

Values reported when a predicted defect has been detected:

Cylinder Low register: F4h

Cylinder High register: 2Ch

STANDBY (E2h)

This command causes the device to enter the Standby mode. If the Count field is non-zero then the Standby timer shall be enabled. The value in the Count field shall be used to determine the time programmed into the Standby timer. If the Count field is zero then the Standby timer is disabled.

STANDBY IMMEDIATE (E0h)

This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately.

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WRITE BUFFER (E8h)

This command enables the host to write the contents of one 512-byte block of data to the device's buffer. The READ BUFFER and WRITE BUFFER commands shall be synchronized within the device such that sequential WRITE BUFFER and READ BUFFER commands access the same bytes within the buffer.

WRITE DMA (CAh)

Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE DMA EXT (35h)

48-bit feature set mandatory command. Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE DMA FUA EXT (3Dh)

48-bit feature set mandatory command. This command provides the same function as the WRITE DMA EXT command except that regardless of whether volatile and/or non-volatile write caching in the device is enabled or not, the user data shall be written to non-volatile media before command completion is reported.

WRITE FPDMA QUEUED (61h)

NCQ feature set mandatory 48-bit command. This command causes data to be transferred from the host to the device.

WRITE LOG EXT (3Fh)

This command writes a specified number of 512 byte blocks of data to the specified log.

WRITE MULTIPLE (C5h)

This command writes the number of logical sectors specified in the Count field. The number of logical sectors per DRQ data block is defined by the content of IDENTIFY DEVICE data word 59. If the number of requested logical sectors is not evenly divisible by the DRQ data block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n logical sectors, where:

n = Remainder (Count / DRQ data block count).

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Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the DRQ data block or partial DRQ data block is transferred. The command ends with the logical sector in error, even if the error was in the middle of a DRQ data block. Subsequent DRQ data blocks are not transferred in the event of an error.

The contents of the Command Structure following the transfer of a DRQ data block that had a logical sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. If IDENTIFY DEVICE data word 59 bit 8 is cleared to zero or IDENTIFY DEVICE data word 59 bits (7:0) are set to zero, and a WRITE MULTIPLE command is received by the device, and no successful SET MULTIPLE MODE command has been processed by the device, the device shall return command aborted. A successful SET MULTIPLE MODE command should precede a WRITE MULTIPLE command.

WRITE MULTIPLE EXT (39h)

48-bit feature set mandatory command. This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE MULTIPLE FUA EXT (CEh)

48-bit feature set mandatory command. This command provides the same functionality as the WRITE MULTIPLE EXT command except that regardless of whether volatile and/or non-volatile write caching in the device is enabled or not, the user data shall be written to non-volatile media before command completion is reported.

WRITE SECTOR(S) (30h/31h)

Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify “00h” to write 256 sectors.

WRITE SECTOR(S) EXT (34h)

48-bit feature set mandatory command. Write data to a specified number of sectors (1 to 65536, as specified with the Sector Count register) from the specified address. Specify “00h” to write 65536 sectors.

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WRITE VERIFY (3Ch)

This command is similar to the WRITE SECTOR(S) command, except that each sector is verified before the command is completed.

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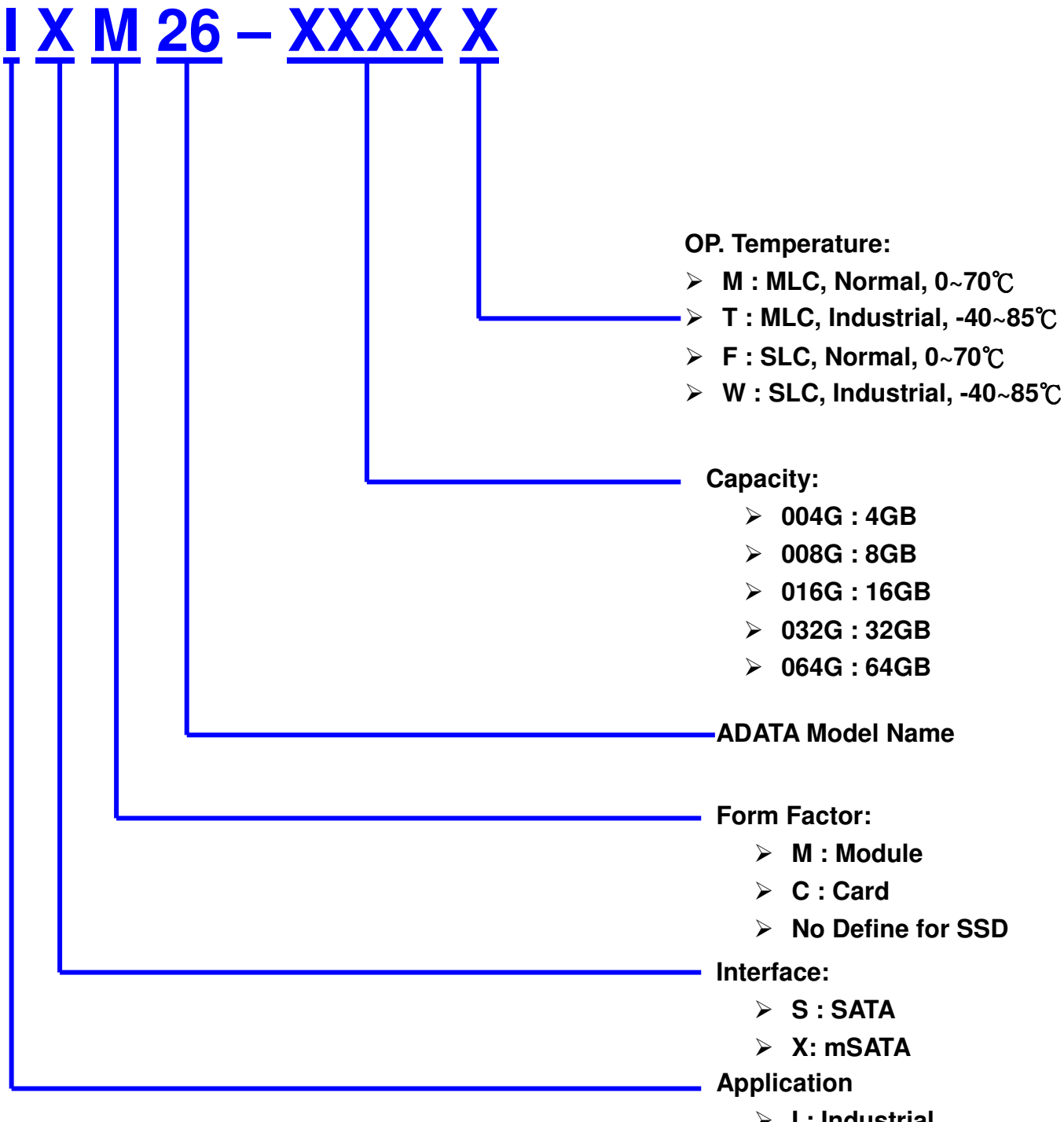
6.0 Order Information

6.1 Model Number



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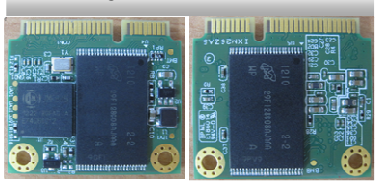
6.2 Packing

Product

IXM26

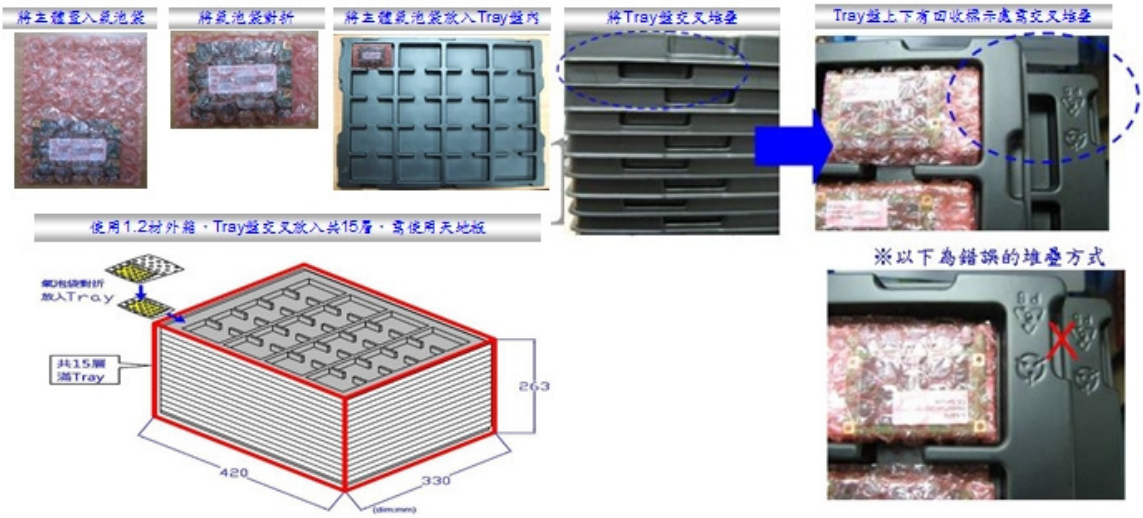


Product with label

IXM26 : Label Sample

Bare machine packing way

將PCBA主體放入氣泡袋，並向下對折，使用黑色Tray盤，將裝好主體的氣泡袋放入Tray盤，每層可放入20pcs，使用1.2材紙箱，先在紙箱中放入一片天地板，每箱可放入15個Tray盤，每層Tray盤需交叉堆疊置入，滿箱共計300pcs，滿箱後需再放上一片天地板。

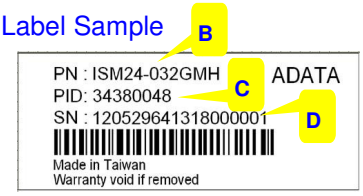


Attachment

Printing Coding Rule

A.(Model/Capacity)	Flash Type & No.	B.(PN)	C.(PID)	D.(SN)	E.(Op. Temp.)
IXM26(F)-1GB	SLC	IXM26-001GF	As SO	As below	0~70℃
IXM26(F)-2GB	SLC	IXM26-002GF			
IXM26(F)-4GB	SLC	IXM26-004GF			
IXM26(F)-8GB	SLC	IXM26-008GF			
IXM26(F)-16GB	SLC	IXM26-016GF			
IXM26(F)-32GB	SLC	IXM26-032GF			
IXM26(M)-4GB	MLC	IXM26-004GM	As SO	As below	0~70℃
IXM26(M)-8GB	MLC	IXM26-008GM			
IXM26(M)-16GB	MLC	IXM26-016GM			
IXM26(M)-32GB	MLC	IXM26-032GM			
IXM26(W)-1GB	SLC	IXM26-001GW	As SO	As below	-40~+85℃
IXM26(W)-2GB	SLC	IXM26-002GW			
IXM26(W)-4GB	SLC	IXM26-004GW			
IXM26(W)-8GB	SLC	IXM26-008GW			
IXM26(W)-16GB	SLC	IXM26-016GW			
IXM26(W)-32GB	SLC	IXM26-032GW			
IXM26(T)-4GB	MLC	IXM26-004GT	As SO	As below	-40~+85℃
IXM26(T)-8GB	MLC	IXM26-008GT			
IXM26(T)-16GB	MLC	IXM26-016GT			
IXM26(T)-32GB	MLC	IXM26-032GT			

Label Sample



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Definition for internal and external S/N

EX: 120529641318000001 (Total 18 codes)

Code	1-8	9-10	11-12	13	14-18
Definition	WIP No.	Year	Week	Product Condition	Counting No.
Example	12052964	13	18	0	00001

Explanation:

1.) Code 1-8: ADATA internal WIP No., total 8 numbers.

2.) Code 9-10: Produced year, 2013=13, 2014=14……

3.) Code 11-12: Produced week

4.) Code 13: Product condition and for RMA used. New finished goods: 0, first time of RMA: 1; Second time of RMA: 2, and such like……

Code 14-18: Serial No. by decimal counting method. Total 5 numbers. And, it will begin from 00001 per each new WIP.

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